Web Results **1** - **10** of about **19,600** for **domain crossing signals + period + random delay + flip-flop**. (**0.66** s

EETimes.com - Clock **domain** modeling is essential in high density ...
All clock **domain crossing** logic should be contained in the bus adapter module. ... naturally introduces a one or two receive clock **period delay**, ...
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Because the synchronizer imposes a two receive clock **delay** and because at ... **domain cr ssing** of the pointers and read/write **signals**. ...
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Semiconductor device for **domain crossing** - Patent 6980479
a **domain crossing** sensing block in response to a operation mode **signal**, first and second **delay** locked loop (DLL) clock **signals** and a CAS latency for ...
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clock **period**. Assume that. is the **delay** time of the ith. **delay** cell, ... PD, implemented by a current-mode-logic D-**flip-flop** (CML ...
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Since all flops are clocked by the same clock **signal**, all logic paths have the same worstcase **delay** requirements, which is clock **period** minus **flipflop** ...
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De-rate > the Tco of the **domain crossing** FFs by some multiple, say 6, of the unrouted > **delay**. Then set up constraints like this: > > TIMESPEC TSSync = FROM ...
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Clock **domain** modeling is essential in high density SoC design
Applying synchronizers is further complicated by **domain crossing** vectors where all bits of ... naturally introduces a one or two receive clock **period delay**, ...
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Using **delay** - Patent Storm
A method for distributing clocks to **flip-flop** circuits which constitute a logic ... The **signal** phase shifting circuit includes a reference **signal period** ...
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[PDF] Chapter 12. DE **Domain**
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Flip Fl p. T. Clk. Q. Q'. Specific to the DE **Domain** ... counting process) through two channels with **random delay**, and. merge the channel outputs. sampler ...
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